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| 浙江大学信息与电子工程学院 | **集成电路原理与设计** | 2023年11月 |
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**Exercise 5**

Table 5.1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | Typical Parameter Value | |  |
| Parameter Symbol | Parameter Description | n-Channel | p-Channel | Units |
| VT0 | Threshold voltage(VBS=0) | 0.7 | -0.8 | V |
| K | Transconductance parameter(in saturation) | 134 | 50 | μA/V2 |
| γ | Bulk threshold parameter | 0.45 | 0.4 | V1/2 |
| λ | Channel length modulation parameter | 0.1 | 0.2 | V-1 |
| 2|ϕF| | Surface potential at strong inversion | 0.9 | 0.8 | V |

* 1. Calculate the output resistance and the minimum output voltage, while maintaining all devices in saturation, for the circuits shown in Figure 5.1. Assume that *i*OUT is actually 10μA. Use Table 5.1 for device model information. Vbs=0 V.



Fig 5.1

**Answer:**

？

1. A reference circuit is shown in figure 5.2, assume that (W/L)1=(W/L)2= (W/L)3=4, (W/L)4=1, please calculate the symbolic expression of VREF.（已知各管处于饱和区且各管阈值电压为Vt）



Figure 5.2

**Answer:**

1. As the circuits shown in Figure 5.3, *IREF*=0.3mA and *γ*=0. Using the model parameters in Table 5.1,

(a) Calculatethe voltage *Vb* when *VX*=*VY*.

(b) If Vb is 100mV smaller than the value in (a), calculate the deviation of Iout from 300μA.

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Figure 5.3

**Answer:**

1. 注意如何推导此步
2. Design M3 and M4 of Figure 5.4(a) so that the output characteristics are identical to the circuit shown in Figure 5.4(b). It is desired that *i*OUT is ideally 10uA.

 

1. (b)

Figure 5.4

**Answer:**

In（b），

In（a）